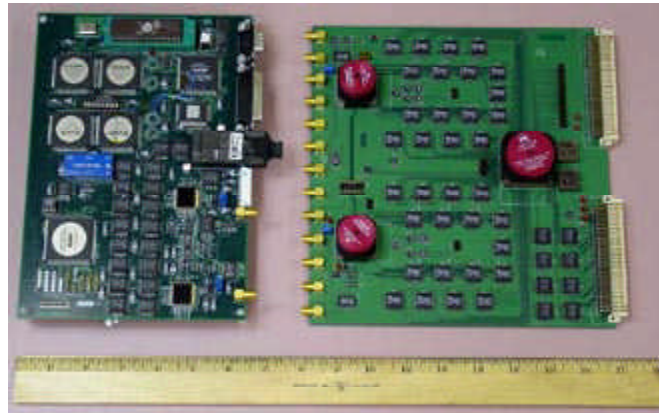


# 622-Mbps Orthogonal Frequency Division Multiplexing (OFDM) Digital Modem Implemented



*622-Mbps OFDM modulator board and OFDM demodulator front-end board.*

Future generation space communications systems feature significantly higher data rates and relatively smaller frequency spectrum allocations than systems currently deployed. This requires the application of bandwidth- and power-efficient signal transmission techniques. There are a number of approaches to implementing such techniques, including analog, digital, mixed-signal, single-channel, or multichannel systems. In general, the digital implementations offer more advantages; however, a fully digital implementation is very difficult because of the very high clock speeds required. Multichannel techniques are used to reduce the sampling rate. One such technique, multicarrier modulation, divides the data into a number of low-rate channels that are stacked in frequency. Orthogonal frequency division multiplexing (OFDM), a form of multicarrier modulation, is being proposed for numerous systems, including mobile wireless and digital subscriber link communication systems.

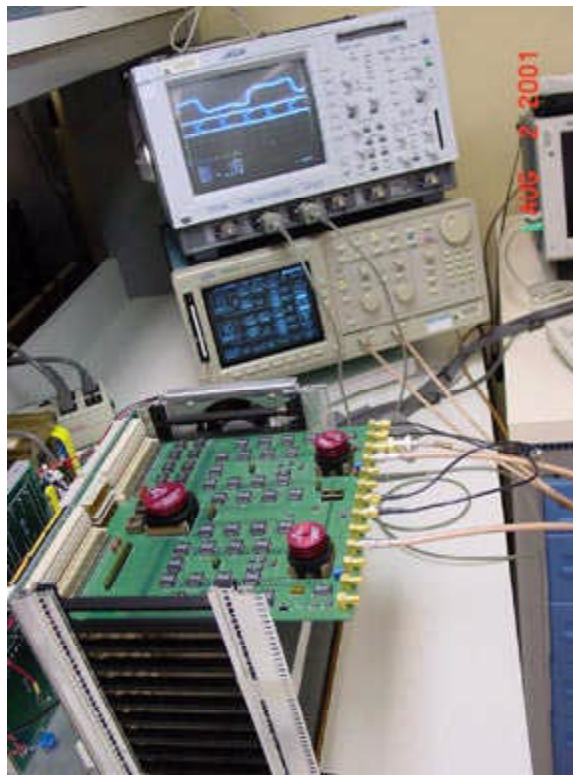
In response to this challenge, NASA Glenn Research Center's Communication Technology Division has developed an OFDM digital modem (modulator and demodulator) with an aggregate information throughput of 622 Mbps. The basic OFDM waveform is constructed by dividing an incoming data stream into four channels, each using either 16-ary quadrature amplitude modulation (16-QAM) or 8-phase shift keying (8-PSK). An efficient implementation for an OFDM architecture is being achieved using the combination of a discrete Fourier transform (DFT) at the transmitter to digitally stack the individual carriers, inverse DFT at the receiver to perform the frequency translations, and a polyphase filter to facilitate the pulse shaping.

One benefit is already evident. Because of the orthogonality of the signals, the four separate channels overlap in frequency without interfering with each other, thus reducing the system bandwidth by up to 38 percent. In addition, Glenn's researchers are working to

reduce size, weight, and power while increasing throughput over state-of-the-art technology. Depending on the chosen modulation scheme, power savings of about 3 dB or more may be realized.

The OFDM modulator board consists of a microcontroller unit, a data interface, four commercial application-specific integrated circuit (ASIC) digital modulator/encoder chips, a phased lock loop, an eight-point DFT, an eight-sample polyphase filter, a high-speed multiplexer, and two digital-to-analog converters. The microcontroller unit, along with the data interface unit, divides data into four parallel channels to allow data processing at a much lower rate. It selects various modulation and coding schemes from ASIC modulator/encoder chips. The phased lock loop provides various clocks suitable for the selected modulation scheme. An eight-point complex DFT and an eight-sample polyphase filter are used to reject aliases when the signal is converted to the analog domain. This direct implementation requires filtering each channel at the sample rate and performing the DFT at the sample rate. The number of computations is greatly reduced by moving the filter function after the DFT and distributing it among the channels.

Demodulation of the OFDM signal requires the implementation of analog-to-digital converters, a high-speed demultiplexer, an eight-sample polyphase filter, an eight-point inverse DFT, a symbol synchronizer, and four single-channel demodulator/decoders. The OFDM demodulator was designed in-house at Glenn and built on an eight-layer VME (VersaModule Eurocard) compatible printed circuit board.



*OFDM demodulator front-end board test setups.*

## **Bibliography**

Kifle, Muli; Andro, Monty; and Vanderaar, Mark J.: An OFDM System Using Polyphase Filter and DFT Architecture for Very High Data Rate Applications. NASA/TM-2001-210813, 2001.

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